UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,292	04/27/2004	Robert J. Allen	BUR920030135US1	3291

29154 7590 09/26/2006

FREDERICK W. GIBB, III
GIBB INTELLECTUAL PROPERTY LAW FIRM, LLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER	
LAM, NELSON C	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 09/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.**	**Applicant(s)**	
	10/709,292	ALLEN ET AL.	
	Examiner	**Art Unit**	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/24/2004*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication on 04/27/2004. Application 10/709,292 has been examined. In the examination of 10/709,292, claims 1-36 are pending.

Claim Objections

2. Claims 13-17, 19-23, 25-29 and 32-36 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The claim numbering is incorrect, e.g., claim 13 is dependent on claim 12 instead of claim 15.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the **first** paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 18-23 are rejected under 35 U.S.C. 112, first paragraph**, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not use or describe the term "service". For examination purposes, the term "service" is interpreted as method.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-36 are rejected under 35 U.S.C. 102(e)** as being anticipated by Papadopoulou et al. (US Patent No. 6,178,539).

As per **claim 1**, Papadopoulou discloses a method of calculating critical area in an integrated circuit design, said method comprising:

inputting an integrated circuit design (Fig. 22, #10; col. 3, line 66-67; col. 8, line 17-20; col. 22, line 20-25);

associating variables with the positions of edges in said integrated circuit design (col. 3, line 6-35; Fig. 7; col. 9, line 8-30); and

associating cost functions of said variables with spacing between said edges in said integrated circuit design (col. 3, line 6-35; col. 3, line 44-67; where the defect density function is a cost function);

wherein said cost functions calculate critical area contributions as the positions and length of said edges in said integrated circuit design change, and wherein said critical area contributions comprise a measure of electrical fault characteristics of said

spacing between said edges in said integrated circuit design (col. 3, line 6-35; col. 3, line 44-67; col. 7, line 60 to col. 8, line 16).

As per **claim 2**, Papadopoulou discloses the method in claim 1, wherein said process of associating said cost functions comprises mapping points in said spacing between said edges in said integrated circuit design up points triggers an electrical fault between said edges into when the size of defects located at said integrated circuit design, wherein said mapping forms Voronoi cells (Abstract; Fig. 6; col. 7, line 24 to col. 8, line 16).

As per **claim 3**, Papadopoulou discloses the method in claim 2, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables (col. 3, line 6-35; col. 3, line 44-67; col. 9, line 1-5; col. 13, line 55 to col. 14, line 3).

As per **claim 4**, Papadopoulou discloses the method in claim 1, wherein said process of associating said cost functions further comprises identifying Voronoi bisectors where Voronoi cells meet (col. 6, line 41-54; col. 11, line 36-49; col. 13, line 8-18).

As per **claim 5**, Papadopoulou discloses the method in claim 4, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors (Figs. 1-2; col. 5, line 66 to col. 6, line 8); and wherein said vertices are defined in terms of said variables (col. 5, line 66 to col. 6, line 33).

As per **claim 6**, Papadopoulou discloses a method of optimizing critical area in an integrated circuit design, said method comprising:

a) inputting an initial integrated circuit design (Fig. 22, #10; col. 3, line 66-67; col. 8, line 17-20; col. 22, line 20-25);

b) associating variables with the positions of edges in said integrated circuit design (col. 3, line 6-35; Fig. 7; col. 9, line 8-30);

c) associating cost functions of said variables with spacing between said edges in said integrated circuit design (col. 3, line 6-35; col. 3, line 44-67; where the defect density function is a cost function);

d) optimizing said positions and length of said edges in said integrated circuit design to reduce critical area contribution cost in a first direction across said integrated circuit design to produce a revised integrated circuit design (col. 3, line 6-35; col. 7, line 60 to col. 8, line 16); and

e) repeating steps b-d with said revised integrated circuit design in a second direction (col. 3, line 44-67).

As per **claim 7**, Papadopoulou discloses the method in claim 6, wherein said process of associating said cost functions comprises mapping points in said spacing between said edges in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges in said integrated circuit design, wherein said mapping forms Voronoi cells (Abstract; Fig. 6; col. 7, line 24 to col. 8, line 16).

As per **claim 8**, Papadopoulou discloses the method in claim 7, wherein said process of associating said cost functions further comprises using a normal vector

representing said Voronoi cells defined in terms of said variables (col. 3, line 6-35; col. 3, line 44-67; col. 9, line 1-5; col. 13, line 55 to col. 14, line 3).

As per **claim 9**, Papadopoulou discloses the method in claim 6, wherein said process of associating said cost functions further comprises identifying Voronoi bisectors where Voronoi cells meet (col. 6, line 41-54; col. 11, line 36-49; col. 13, line 8-18).

As per **claim 10**, Papadopoulou discloses the method in claim 9, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors (Figs. 1-2; col. 5, line 66 to col. 6, line 8); and

wherein said vertices are defined in terms of said variables (col. 5, line 66 to col. 6, line 33).

As per **claim 11**, Papadopoulou discloses the method in claim 10, wherein said cost function calculates critical area contributions of said Voronoi bisectors as said variables change as the layout of said integrated circuit design changes (col. 11, line 3-35).

As per **claim 12**, Papadopoulou discloses a method of optimizing critical area in an integrated circuit design, said method comprising:

a) inputting an initial integrated circuit design (Fig. 22, #10; col. 3, line 66-67; col. 8, line 17-20; col. 22, line 20-25);

b) associating variables with the positions of edges in said integrated circuit design (col. 3, line 6-35; Fig. 7; col. 9, line 8-30);

c) associating spacing between said edges in said integrated circuit design, wherein said cost functions are in terms of critical area contributions (col. 3, line 6-35; col. 3, line 44-67; where the defect density function is a cost function), and wherein said critical cost functions of said variables with area contributions comprise a measure of electrical fault characteristics of said spacing between said edges in said integrated circuit design (col. 3, line 6-35; col. 3, line 44-67; col. 7, line 60 to col. 8, line 16);

d) optimizing said positions and lengths of said edges in said integrated circuit design to reduce critical area contribution cost in a first direction across said integrated circuit design to produce a revised integrated circuit design (col. 3, line 6-35; col. 7, line 60 to col. 8, line 16); and

e) repeating steps b-d with said circuit design in a revised integrated second direction (col. 3, line 44-67).

As per **claim 13**, Papadopoulou discloses the method in claim 15, wherein said process of associating said cost functions comprises in said spacing mapping points between said edges in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges in said integrated circuit design, wherein said mapping forms Voronoi cells (Abstract; Fig. 6; col. 7, line 24 to col. 8, line 16).

As per **claim 14**, Papadopoulou discloses the method in claim 16, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables (col. 3, line 6-35; col. 3, line 44-67; col. 9, line 1-5; col. 13, line 55 to col. 14, line 3).

As per **claim 15**, Papadopoulou discloses the method in claim 15, wherein said process of associating said cost functions further comprises identifying Voronoi bisectors where Voronoi cells meet (col. 6, line 41-54; col. 11, line 36-49; col. 13, line 8-18).

As per **claim 16**, Papadopoulou discloses the method in claim 18, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors (Figs. 1-2; col. 5, line 66 to col. 6, line 8); and

wherein said vertices are defined in terms of said variables (col. 5, line 66 to col. 6, line 33).

As per **claim 17**, Papadopoulou discloses the method in claim 19, wherein said cost function calculates critical area contributions of said Voronoi bisectors as said variables change as the layout of said integrated circuit design changes (col. 11, line 3-35).

As per **claim 18**, Papadopoulou discloses a service (Fig. 22; col. 22, line 15-23) for calculating critical area in an integrated circuit design, inputting said service comprising:

an integrated circuit design (Fig. 22, #10; col. 3, line 66-67; col. 8, line 17-20; col. 22, line 20-25);

associating variables with the positions of edges in said integrated circuit design (col. 3, line 6-35; Fig. 7; col. 9, line 8-30); and

associating cost functions of said variables with spacing between said edges in said integrated circuit design (col. 3, line 6-35; col. 3, line 44-67; where the defect density function is a cost function);

wherein said cost functions are in terms of critical area contributions (col. 3, line 6-35; col. 7, line 60 to col. 8, line 16), and wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges in said integrated circuit design (col. 3, line 6-35; col. 3, line 44-67; col. 7, line 60 to col. 8, line 16).

As per **claim 19**, Papadopoulou discloses the service in claim 22, wherein said process mapping points of associating said cost functions comprises in said spacing between said edges in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges in said integrated circuit design, wherein said mapping forms Voronoi cells (Abstract; Fig. 6; col. 7, line 24 to col. 8, line 16).

As per **claim 20**, Papadopoulou discloses the service in claim 23, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables (col. 3, line 6-35; col. 3, line 44-67; col. 9, line 1-5; col. 13, line 55 to col. 14, line 3).

As per **claim 21**, Papadopoulou discloses the service in claim 22, wherein said process of associating said cost functions further comprises identifying Voronoi bisectors where Voronoi cells meet (col. 6, line 41-54; col. 11, line 36-49; col. 13, line 8-18).

As per **claim 22**, Papadopoulou discloses the service in claim 2 5, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors (Figs. 1-2; col. 5, line 66 to col. 6, line 8); and

wherein said vertices are defined in terms of said variables (col. 5, line 66 to col. 6, line 33).

As per **claim 23**, Papadopoulou discloses the calculates service in claim 26, wherein said cost function critical area contributions of said Voronoi bisectors as said variables change as the layout of said integrated circuit design changes (col. 11, line 3-35).

As per **claim 24**, Papadopoulou discloses a program storage device readable by computer (Fig. 22; col. 22, line 15-23), tangibly embodied a program of instructions executable by said computer for performing a method of calculating critical area in an integrated circuit design, said method comprising:

inputting an integrated circuit design (Fig. 22, #10; col. 3, line 66-67; col. 8, line 17-20; col. 22, line 20-25);

associating variables with the positions of edges in said integrated circuit design (col. 3, line 6-35; Fig. 7; col. 9, line 8-30); and

associating cost functions of said variables with spacing between said edges in said integrated circuit design (col. 3, line 6-35; col. 3, line 44-67; where the defect density function is a cost function);

wherein said cost functions are in terms of critical area contributions (col. 3, line 6-35; col. 7, line 60 to col. 8, line 16); and

wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges in said integrated circuit design (col. 3, line 6-35; col. 3, line 44-67; col. 7, line 60 to col. 8, line 16).

As per **claim 25**, Papadopoulou discloses the program storage device in claim 29, wherein said process of associating said cost functions comprises mapping points in said spacing between said edges in triggers an electrical fault integrated circuit design, said integrated circuit design up to when the size of defects located at said points between said edges in said wherein said mapping forms Voronoi cells (Abstract; Fig. 6; col. 7, line 24 to col. 8, line 16).

As per **claim 26**, Papadopoulou discloses the program storage device in claim 30, wherein said process of associating said cost functions further comprises using a normal vector representing said Voronoi cells defined in terms of said variables (col. 3, line 6-35; col. 3, line 44-67; col. 9, line 1-5; col. 13, line 55 to col. 14, line 3).

As per **claim 27**, Papadopoulou discloses the program storage device in claim 29, wherein said process of associating said cost functions further comprises identifying Voronoi bisectors where Voronoi cells meet (col. 6, line 41-54; col. 11, line 36-49; col. 13, line 8-18).

As per **claim 28**, Papadopoulou discloses the program storage device said Voronoi bisectors are defined by vertices at the ends in claim 32, wherein of said Voronoi bisectors (Figs. 1-2; col. 5, line 66 to col. 6, line 8); and

wherein said vertices are defined in terms of said variables (col. 5, line 66 to col. 6, line 33).

As per **claim 29**, Papadopoulou discloses the program storage device in claim 33, wherein said cost function calculates critical area contributions of said Voronoi bisectors as said variables change as the layout of said integrated circuit design changes (col. 11, line 3-35).

As per **claim 30**, Papadopoulou discloses a system (col. 3, line 36-40; Fig. 22; col. 22, line 15-23) for calculating critical area in an integrated circuit design, said system comprising:

means for inputting an integrated circuit design (Fig. 22, #10; col. 3, line 66-67; col. 8, line 17-20; col. 22, line 20-25);

means for associating variables with the positions of edges in said integrated circuit design (col. 3, line 6-35; Fig. 7; col. 9, line 8-30); and

means for associating cost functions of said variables with spacing between said edges in said integrated circuit design (col. 3, line 6-35; col. 3, line 44-67; where the defect density function is a cost function);

wherein said cost functions are in terms of critical area contributions, and wherein said critical area contributions comprise a measure of electrical fault characteristics of said spacing between said edges in said integrated circuit design (col. 3, line 6-35; col. 3, line 44-67; col. 7, line 60 to col. 8, line 16).

As per **claim 31**, Papadopoulou discloses a method of optimizing critical area in an integrated circuit design, said method comprising:

inputting an initial integrated circuit design (Fig. 22, #10; col. 3, line 66-67; col. 8, line 17-20; col. 22, line 20-25);

associating variables with the positions of edges in said integrated circuit design (col. 3, line 6-35; Fig. 7; col. 9, line 8-30);

associating cost functions of said variables with spacing between said edges in design (col. 3, line 6-35; col. 3, line 44-67; where the defect density function is a cost function); and

said integrated circuit optimizing said positions and length of said edges in said integrated circuit design to reduce critical area contribution cost in a first direction across said integrated circuit design to produce a revised integrated circuit design (col. 3, line 6-35; col. 7, line 60 to col. 8, line 16).

As per **claim 32**, Papadopoulou discloses the method in claim 37, wherein said process of associating said cost functions comprises in said spacing mapping points between said edges in said integrated circuit design up to when the size of defects located at said points triggers an electrical fault between said edges in said integrated circuit design, wherein said mapping forms Voronoi cells (Abstract; Fig. 6; col. 7, line 24 to col. 8, line 16).

As per **claim 33**, Papadopoulou discloses the method in claim 38, wherein said cost functions further comprises using a said process of associating normal vector representing said Voronoi cells defined in terms of said variables (col. 3, line 6-35; col. 3, line 44-67; col. 9, line 1-5; col. 13, line 55 to col. 14, line 3).

As per **claim 34**, Papadopoulou discloses the method in claim 37, wherein said process of associating said cost functions further comprises identifying Voronoi

bisectors where Voronoi cells meet (col. 6, line 41-54; col. 11, line 36-49; col. 13, line 8-18).

As per **claim 35**, Papadopoulou discloses the method in claim 40, wherein said Voronoi bisectors are defined by vertices at the ends of said Voronoi bisectors (Figs. 1-2; col. 5, line 66 to col. 6, line 8); and

wherein said vertices are defined in terms of said variables (col. 5, line 66 to col. 6, line 33).

As per **claim 36**, Papadopoulou discloses the method in claim 41, wherein said cost function calculates critical area contributions of said Voronoi bisectors as said variables change as the layout of said integrated circuit design changes (col. 11, line 3-35).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday from 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nelson Lam

Nelson Lam
Assistant Examiner
Art Unit 2825

Jack Chiang
JACK CHIANG
SUPERVISORY PATENT EXAMINER